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(54) RF phase and/or amplitude control device

(57) An RF phase and/or amplitude control device (40) has a digitally controlled attenuator (41) at it input to adjust the overall output level of the output. The device includes an in-phase power divider (43) for splitting up the input signals over two paths (I and Q). The power divided signals in the two paths are further power divided and shifted in relative phase at 180° hybrids (49 and 50). The power divided and phases shifted signals in each path I and Q are selectively switched using switches (51 and 53). The selected and switched output is quadrative combined at a 90° hybrid (55). This provides a single inexpensive device which can provide digitally controlled output signals which are either phase controlled or amplitude controlled or both.

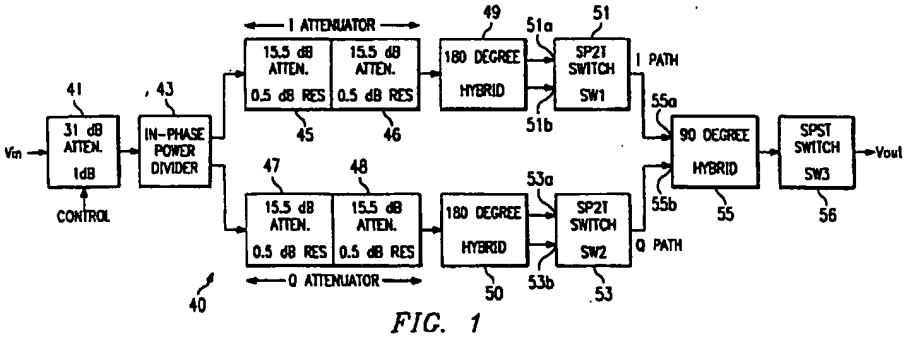

FIG. 1

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Description

TECHNICAL FIELD OF THE INVENTION

This invention relates to RF systems and more particularly to a digitally addressable RF control device for control of an RF signal.

BACKGROUND OF THE INVENTION

Radio frequency signal (RF) phase and amplitude control devices are used in a wide range of applications such as communication systems, radar systems, antenna systems, etc. It is further highly desirable that these RF control devices used for phase and amplitude control be digitally addressable devices. These RF control devices may include ferrite devices (such as ferrite phase shifters, for example) or semiconductor devices. The ferrite devices are expensive and the performance is limited. Semiconductor devices such as varactors, PIN diodes, and transistors are temperature sensitive, and therefore, resolution limited. It is therefore highly desirable to provide a high resolution RF control device for control using low cost elements.

SUMMARY OF THE INVENTION

In accordance with one embodiment of the present invention an improved RF control device for phase shifting and/or amplitude control of an RF signal is provided. The RF control device includes a power divider for power dividing the RF input to provide first and second power divided signals. The power divided signals are separately amplitude controlled by digital control means. The level controlled power divided signals are then quadrature phase combined to provide phase and/or amplitude controlled output signals. This provides a single inexpensive device which can provide digitally controlled output signals which are either phase controlled or amplitude controlled or both.

These and other features of the invention will be apparent to those skilled in the art from the following detailed description of the invention, taken together with the accompanying drawings.

DESCRIPTION OF THE DRAWINGS

The present invention will now be further described, by way of example, with reference to the accompanying drawings in which:

Fig. 1 is a block diagram of an RF control device according to one embodiment of the present invention;
Fig. 2 is a graph of the settings for the device of Fig. 1 where the I path is represented by solid lines and Q path by dashed lines;
Fig. 3 illustrates the phase error using the attenuator setting of Fig. 2;
Fig. 4 illustrates the amplitude variation for the attenuator settings of Fig. 3;
Fig. 5 illustrates the distribution of phase errors for the results shown in Fig. 3;
Fig. 6 illustrates the vector magnitude error distribution for the results shown in Fig. 4; and
Fig. 7 shows the comparison of the digital processor calculated I and Q values with the values determined from an ideal weighter circuit.

DESCRIPTION OF PREFERRED EMBODIMENTS OF THE PRESENT INVENTION

In accordance with an embodiment of the present invention there is provided an RF control device 40 as illustrated in Fig. 1. The RF control device includes an input variable attenuator 41 which is a step attenuator that attenuates in half dB increments from 0 to 31 dB. This attenuator 41 is digitally controlled having nine binary inputs. The attenuator 41 is implemented for example using two cascaded MA/COM AT280 attenuators each having a range of 15.5 dB in 0.5 dB steps. The attenuator 41 adjusts the overall output power level. The output (at A) from the attenuator 41 is power divided by an equal in-phase power divider 43 and applied separately to an I (at B) and a Q (C) path. The in-phase power divider is for example a MA/COM DS-327. A lower cost Wilkinson power divider may also be used. In this particular embodiment, the I path includes 15.5 dB attenuators 45 and 46 cascaded in series. Similarly the Q path has two 15.5 dB attenuators 47 and 48 cascaded in series. These attenuators 45-48 are also digitally controlled by binary inputs. They are also MA/COM T280 attenuators for example. These attenuators are low cost surface mount GaAs (Gallium Arsenide) attenuators. These attenuators can adjust the relative amplitudes of signals in the I and Q paths. The output at D and E are from the separate I and Q attenuators 46 and 48. The output at point D from attenuator 46 is applied to 180° hybrid 49 to produce two equal power (power divided) 180° out of phase shifted signals at 51a and

51b. This 180° hybrid 19 is, for example, MA/COM HH-128 hybrid. This hybrid 19 may also be made at a lower cost using a rat race hybrid in microstrip. Likewise, the output at point E from attenuator 48 is applied to 180° hybrid 50 to produce two equal power signals that are 180° out of phase at 53a and 53b. The hybrid 50 is also on MA/COM HH-128 hybrid, but may be a rat race hybrid. The selected output from points 51a or 51b in path I is applied by a single pole double throw switch 51 to a port 55a of a 90° hybrid 55. This switch, for example, is a MA/COM SW 29. Similarly, the selected output from points 53a or 53b in path Q is applied by single pole double throw switch 53 to the port 55b of 90° hybrid 55. This switch is also, for example, a MA/COM SW29. The 90° hybrid 55, for the example, is a MA/COM JH140. It may be made at a lower cost using a Lange microstrip hybrid coupler or branch line hybrid coupler. The outputs from the I path and the Q path are then combined through the 90° hybrid 55. The output is provided via SPST (single pole double throw switch 56).

The 180° hybrids 49 and 50 followed by SP2T switches 51 and 53 establish which quadrant the vector is in while the 90 degree hybrid, 55, vector combines the I and Q magnitudes orthogonally.

The mathematics of this vector weighter are summarized below and references are to locations shown on the block diagram of Fig. 1. At point A the value is $k_1 * v_{in}$ where $k_1 = 10^{(ATT1/20)}$ and ATT1 (41) is negative dB.

At points B and C,

$$\frac{k_1 * v_{in}}{\sqrt{2}} .$$

At point D,

$$\frac{k_1 * k_2 * v_{in}}{\sqrt{2}}$$

where $k_2 = 10^{((ATT2 + ATT3)/20)}$ and ATT2 (45) and ATT3 (46) are negative.

At point E,

$$\frac{k_1 * k_3 * v_{in}}{\sqrt{2}}$$

where $k_3 = 10^{((ATT4 + ATT5)/20)}$ and ATT4 (47) and ATT5 (48) are negative.

At point 51a(F),

$$\frac{k_1 * k_2 * v_{in}}{2} .$$

At point 51b(G),

$$- \frac{k_1 * k_2 * v_{in}}{2} .$$

At point 53a(H),

$$\frac{k_1 * k_3 * v_{in}}{2} .$$

At point 53b(I),

$$-\frac{k_1 * k_3 * v_{in}}{2}.$$

The selected outputs at point L out of hybrid 55 are:

SW1-1 SW2-1	$\frac{k_1 * k_2 * v_{in}}{2} + j.\frac{k_1 * k_3 * v_{in}}{2}$	Phase = 0 to +90
SW1-1 SW2-2	$\frac{k_1 * k_2 * v_{in}}{2} - j.\frac{k_1 * k_3 * v_{in}}{2}$	Phase = 0 to -90
SW1-2 SW2-1	$-\frac{k_1 * k_2 * v_{in}}{2} + j.\frac{k_1 * k_3 * v_{in}}{2}$	Phase = 90 to 180
SW1- 2 SW2-2	$-\frac{k_1 * k_2 * v_{in}}{2} - j.\frac{k_1 * k_3 * v_{in}}{2}$	Phase -90 to -180

In general,

$$v_{out} = \frac{v_{in} * k_1}{2} \cdot [\pm \cdot k_2 \pm j k_3].$$

An optimization strategy is one where

$$\sqrt{k_2^2 + k_3^2}$$

is between 1 (0dB) and 1.059 (+0.5dB) for k_2 and k_3 varying from 0.02818(-31 dB) to 1(0dB) in 0.5 dB steps, then the ideal loss will be between -5.5 and -6 dB. The actual loss will be greater due to component losses.

The strategy is to minimize the vector magnitude variation with phase while allowing the minimum possible phase step size for 0.5 dB resolution attenuators. Such an algorithm was developed with the absolute minimum phase step size determined to be 0.8 degrees and the worst case magnitude variation equal to 0.5 dB. The 0.8 degrees step size corresponds to approximately 9 bit resolution.

Fig. 2 is a graph of the optimum attenuator setting of ATT2 (45), ATT3 (46), ATT4 (47), and ATT5 (48) for phases from -180 to +180 in 1 degree increments. The switch settings are also shown on Fig. 2. In Fig. 2, SW1-2 is switch 51 providing 51b output, SW2-2 is switch 53 providing 53b output, SW1-1 is switch 51 providing 51a output and SW2-1 is switch 53 providing 53a output. The solid lines is for attenuator settings in path I and the dashed lines is for attenuator setting in path Q.

This device is optimized using two criteria. One was to realize the minimum phase error using 0.5 dB increment sizes of the I attenuators and Q attenuators and using the complete 31 dB range. The other optimization criteria was that the vector length have a maximum variation of 0.5 dB over 360 degrees. The phase error using the attenuator setting of Fig. 2 is shown in Fig. 3. The worst case errors of 1.61 degrees occurs at 0, 90, -90, and 180 degree points however, 96% of the errors are less than 0.8 degrees.

The amplitude variation of vector for the attenuator settings of Fig. 2 is shown in Fig. 4.

Fig. 5 shows the distribution of phase errors for the results shown in Fig. 3. From this graph, about 4% of the errors are greater than 1 degree with the maximum being 1.61 degrees. 96% of the errors are less than 0.8 degrees.

Fig. 6 shows the vector length magnitude error distributions for the results shown in Fig. 4. This shape suggests a uniform distribution of errors about the mean value of +0.217 dB (1.0253 magnitude) with a maximum error of + 0.235 dB about this mean value.

The digital processor will determine an RF phase (ϕ) value and an RF magnitude (k_1) value. The desired phase

angle will be defined from an I and Q value. The vector magnitude will be established by one value, k_1.

The I and Q values will be calculated as follows.

$$I = +1.0253 * COS(\phi)$$

$$Q = +1.0253 * SIN(\phi)$$

where ϕ will be 0 to 90 degrees in 1 degree steps and
where the + or - sign will select the proper quadrant for ϕ.

The vector magnitude will be determined from the following relationship.

$$k_1 = 10^{\left(\frac{attenuation}{20}\right)}$$

where *attenuation* will be from 0 to -31 dB.

A lookup table in RAM (Random Access Memory) will establish the corresponding address to the digital RF vector weighting circuit.

Fig. 7 shows the comparison of the digital processor calculated I and Q values with the values determined from the ideal vector weighter circuit.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention.

Claims

1. An RF control device comprising:

   a power divider for power dividing an RF input signal to provide separate first and second power divided signals;
   an amplitude controller coupled to said power divider for digitally controlling the amplitude of the first and second power divided signals; and
   a combiner coupled to controller for quadrature combining said first and second power divided signals to provide at least one digitally controlled output signal which is phase controlled or amplitude controlled.

2. The RF control device of Claim 1 wherein said combiner is arranged for separately combining said power divided signals and includes a 90° hybrid.

3. The RF control device of Claim 1 or Claim 2, wherein said controller for controlling the amplitude of the first and second power divided signals includes digitally controlled attenuators.

4. The RF control device of any of Claims 1 to 3, wherein said controller for controlling the amplitude of the first and second power divided signals includes a separate control means for said first and second power divided signals where each of said separate control means includes an output of phase power divider and a switch to apply one of the out of phase signals to said combiner.

5. A digitally adjustable RF control device for controlling the phase and/or amplitude and an RF input signal comprising:

   an in-phase power divider responsive to said RF input signals for power dividing said RF signal to provide first and second power divided signals;
   digitally controlled amplitude control means coupled to said power divider and responsive to said first and second power divided signals for controlling the amplitude of said first and second power divided signals;
   a first 180 degree hybrid coupled to said amplitude control means and responsive to said first power divided signals for providing third and fourth power divided signals where said third power divided signals are 180 degrees out of phase with respect to said fourth power divided signals;

a second 180 degree hybrid coupled to said amplitude control means and responsive to said second power divided signals for providing fifth and sixth power divided signals where said fifth power divided signals are 180 degrees out of phase with respect to said sixth power divided signals;

first switch means coupled to said first 180 degree hybrid for selectively providing said third or said fourth power divided signals;

second switch means coupled to said second 180 degree hybrid for selectively providing said fifth or said sixth power divided signals; and

a 90 degree hybrid coupled to said first and said second switch means for combining said selected third or fourth power divided signals from said first switch means and said fifth or sixth power divided signal from said second switch means to provide an RF output signals which is the vector sum of said signals from said first switch means shifted 90 degrees relative to said signal from said second switch means.

6. An RF control device comprising:

first power divider means for power dividing RF input signal to provide first and second power divided signals;

amplitude control means coupled to said first power divider means for controlling the amplitude of said first and second power divided signals;

second power divider means coupled to said amplitude control means and responsive to said first power divided signals for providing third and fourth power divided signals of opposite phase;

third power divider means coupled to said amplitude control means and responsive to said second power divided signals for providing fifth and sixth power divided signals of opposite phase;

switch means coupled to said third and fourth power divider means for selectively providing third or fourth power divided signals at one switch output and fifth or sixth power divided signals at a second switch output; and

quadrature combiner means coupled to said first and second switch outputs for combining signal from first and second inputs at phase quadrature whereby the phase of the output signal is dependent on the selective position of the switch means and the relative amplitudes of the third, fourth, fifth and sixth power divided signals.

7. The RF device of Claim 6, further comprising a RF input terminal and preliminary amplitude control means coupled between said RF input terminal and said first power divider means for controlling the overall input amplitude to said RF device.

8. The device of any preceding Claim, wherein said output signal is both phase and amplitude controlled.

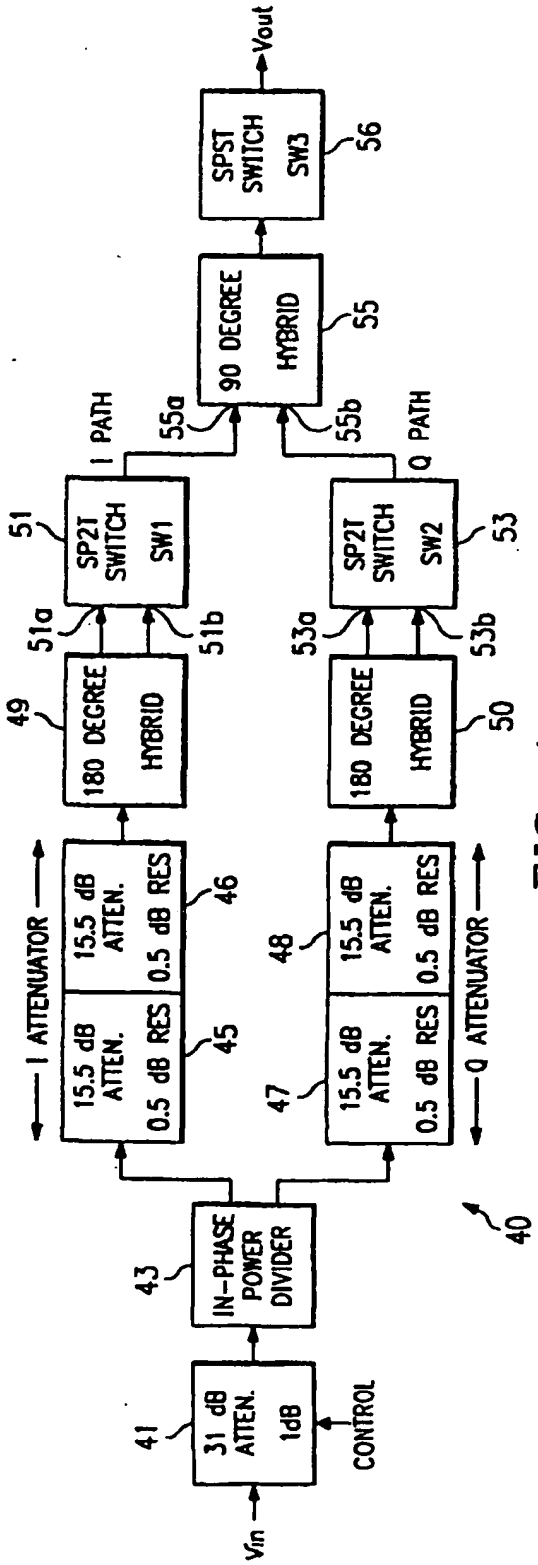
Vin
31 dB ATTEN. 1dB
41
CONTROL
IN-PHASE POWER DIVIDER
43
I ATTENUATOR
15.5 dB ATTEN.
0.5 dB RES
45
15.5 dB ATTEN.
0.5 dB RES
46
Q ATTENUATOR
15.5 dB ATTEN.
0.5 dB RES
47
15.5 dB ATTEN.
0.5 dB RES
48
180 DEGREE HYBRID
49
180 DEGREE HYBRID
50
SP2T SWITCH SW1
51
51a
51b
SP2T SWITCH SW2
53
53a
53b
I PATH
Q PATH
90 DEGREE HYBRID
55
55a
55b
SPST SWITCH SW3
56
Vout
40

FIG. 1

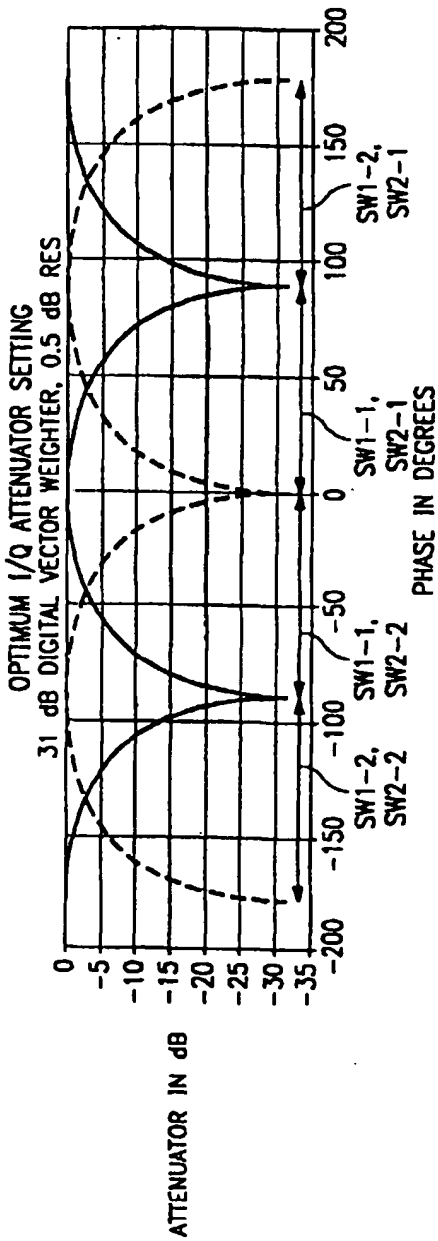
OPTIMUM I/Q ATTENUATOR SETTING
31 dB DIGITAL VECTOR WEIGHTER, 0.5 dB RES
ATTENUATOR IN dB
0
-5
-10
-15
-20
-25
-30
-35
-200
-150
-100
-50
0
50
100
150
200
SW1-2, SW2-2
SW1-1, SW2-2
SW1-1, SW2-1
SW1-2, SW2-1
PHASE IN DEGREES
I ATTENUATOR
Q ATTENUATOR

FIG. 2

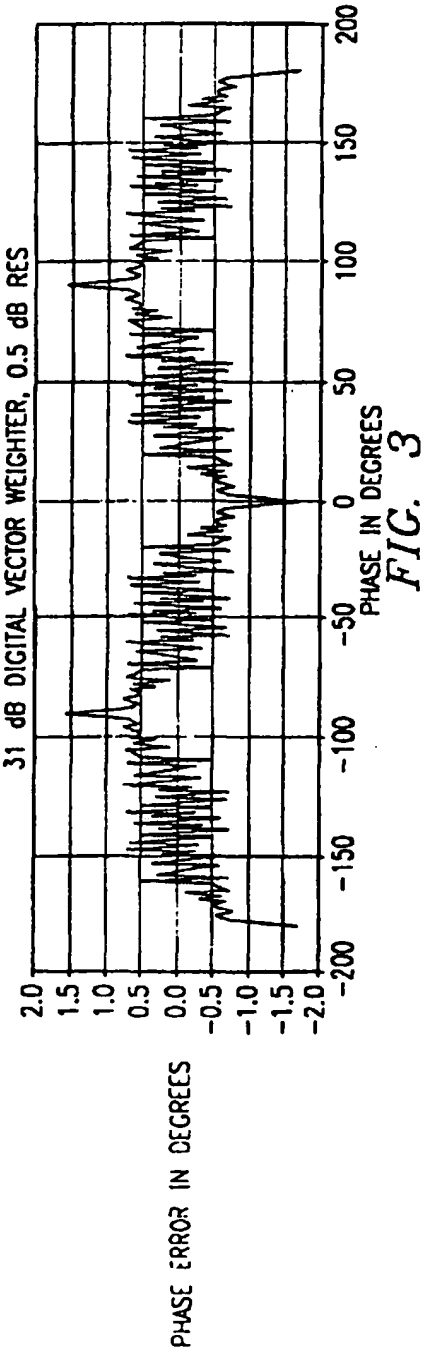
PHASE ERROR FOR 1 DEGREE INCREMENTS
31 dB DIGITAL VECTOR WEIGHTER, 0.5 dB RES
PHASE ERROR IN DEGREES
2.0
1.5
1.0
0.5
0.0
-0.5
-1.0
-1.5
-2.0
-200
-150
-100
-50
0
50
100
150
200
PHASE IN DEGREES

FIG. 3

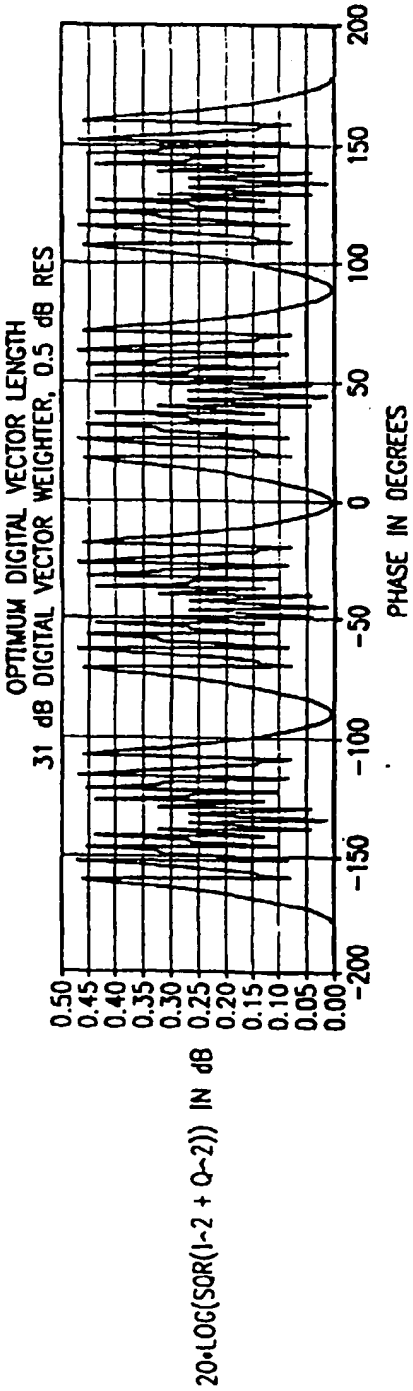
OPTIMUM DIGITAL VECTOR LENGTH
31 dB DIGITAL VECTOR WEIGHTER, 0.5 dB RES
20•LOG(SQR(I^2 + Q^2)) IN dB
0.50
0.45
0.40
0.35
0.30
0.25
0.20
0.15
0.10
0.05
0.00
-200
-150
-100
-50
0
50
100
150
200
PHASE IN DEGREES

FIG. 4

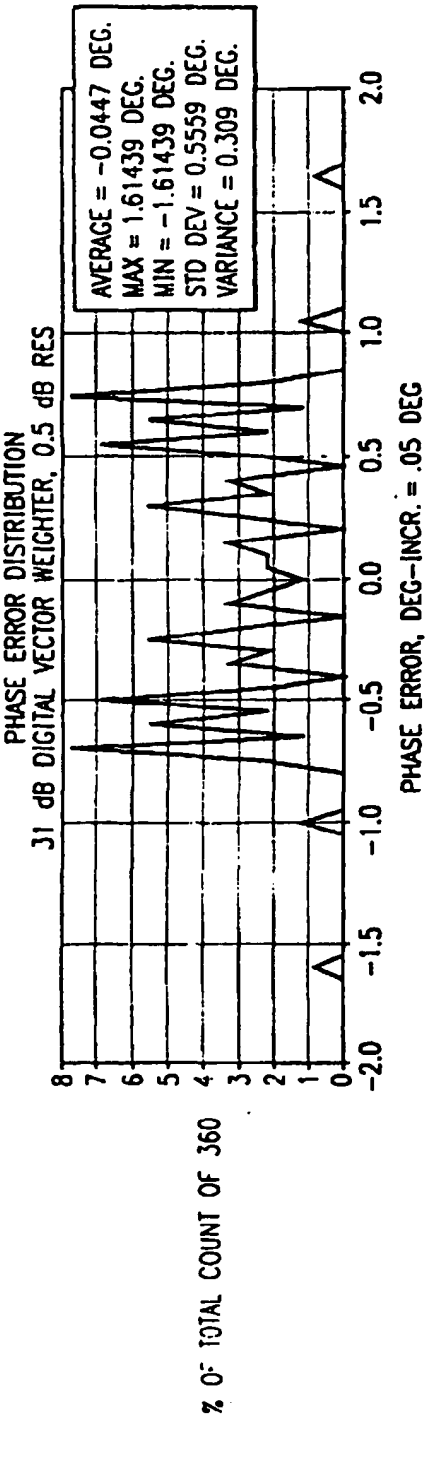
PHASE ERROR DISTRIBUTION
31 dB DIGITAL VECTOR WEIGHTER, 0.5 dB RES
AVERAGE = -0.0447 DEG.
MAX = 1.61439 DEG.
MIN = -1.61439 DEG.
STD DEV = 0.5559 DEG.
VARIANCE = 0.309 DEG.
% OF TOTAL COUNT OF 360
8
7
6
5
4
3
2
1
0
-2.0
-1.5
-1.0
-0.5
0.0
0.5
1.0
1.5
2.0
PHASE ERROR, DEG-INCR. = .05 DEG

FIG. 5

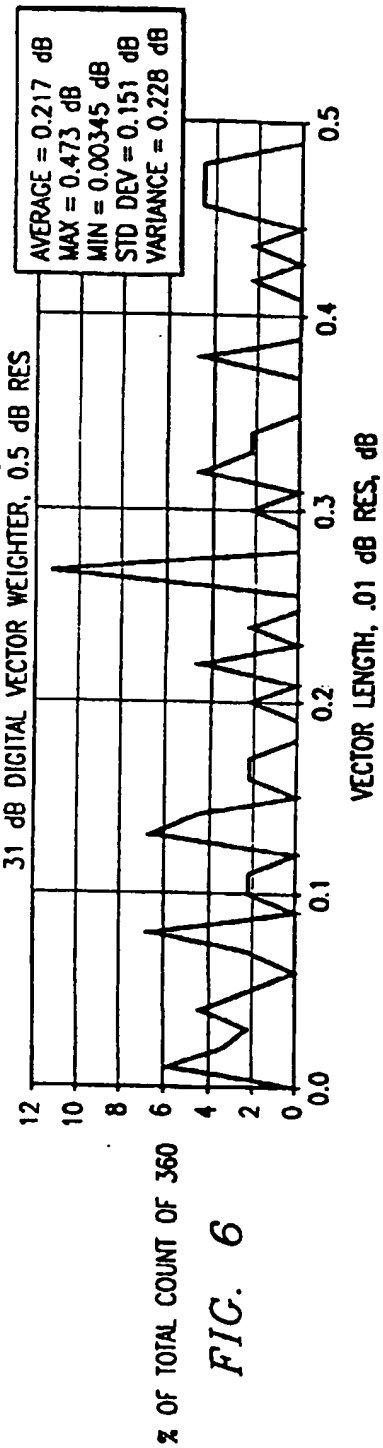
VECTOR LENGTH DISTRIBUTION
31 dB DIGITAL VECTOR WEIGHTER, 0.5 dB RES
AVERAGE = 0.217 dB
MAX = 0.473 dB
MIN = 0.00345 dB
STD DEV = 0.151 dB
VARIANCE = 0.228 dB
% OF TOTAL COUNT OF 360
VECTOR LENGTH, .01 dB RES, dB
0
2
4
6
8
10
12
0.0
0.1
0.2
0.3
0.4
0.5

FIG. 6

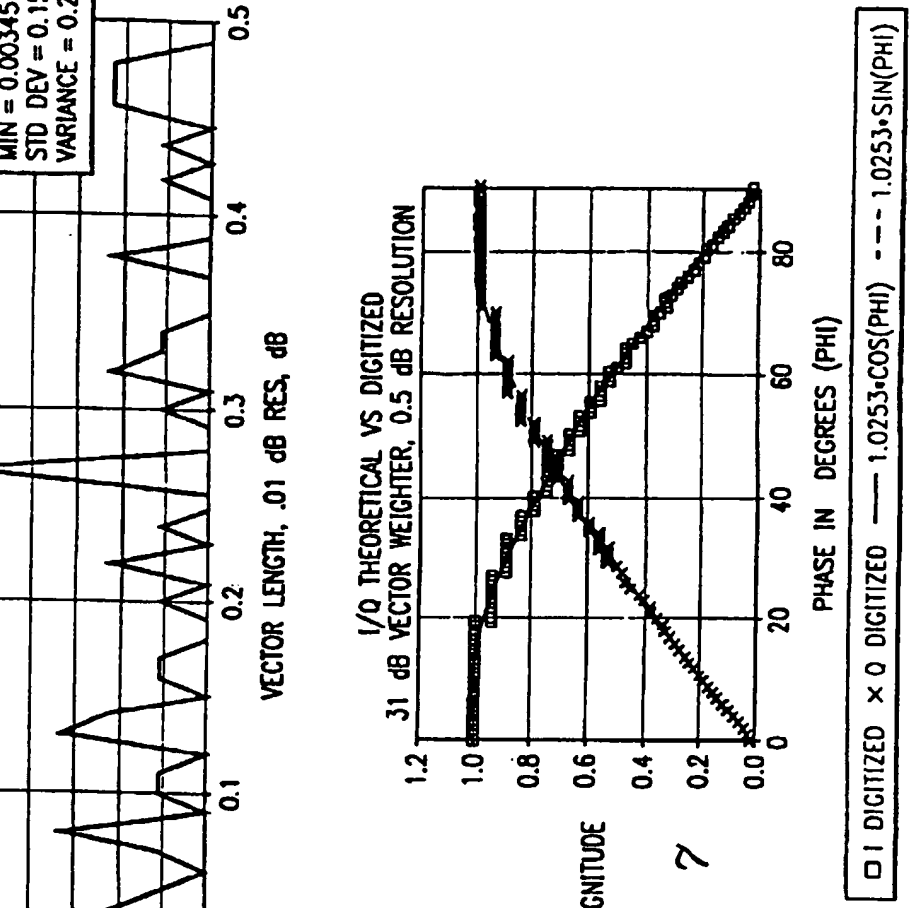
I/Q THEORETICAL VS DIGITIZED
31 dB VECTOR WEIGHTER, 0.5 dB RESOLUTION
I OR Q MAGNITUDE
PHASE IN DEGREES (PHI)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
0
20
40
60
80
I DIGITIZED × Q DIGITIZED
1.0253•COS(PHI)
1.0253•SIN(PHI)

FIG. 7